CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method for making an integrated circuit capacitor comprising:

forming a bottom electrode over a substrate;

forming a tantalum pentoxide layer over said bottom electrode;

annealing said tantalum pentoxide layer in a nitrogen atmosphere;

annealing said tantalum pentoxide layer in an oxygen containing atmosphere; and

forming an upper electrode over said tantalum pentoxide layer.

2. A method of claim 1 wherein said oxygen containing atmosphere is an ozone atmosphere.

3. A method of claim 2 wherein an oxidizable material is provided over said substrate, said ozone atmosphere anneal being performed at a temperature which does not increase the resistance of said oxidizable material by more than about 50% over its initial resistance.

4. A method of claim 1 wherein said nitrogen anneal precedes said oxygen containing atmosphere anneal.

5. A method of claim 1 wherein said oxygen containing atmosphere anneal precedes said nitrogen anneal.

6. A method of claim 3 further comprising forming diffusion barrier between said oxidizable material and said bottom electrode.

7. A method of claim 6 wherein said diffusion barrier comprises tantalum nitride.

8. A method of claim 6 wherein said diffusion barrier comprises tantalum silicon nitride.

9. A method of claim 6 wherein said diffusion barrier comprises titanium nitride.

10. A method of claim 1 wherein said bottom electrode is formed by chemical vapor deposition.

11. A method of claim 1 wherein said bottom electrode comprises platinum.

12. A method of claim 1 wherein said bottom electrode comprises rhodium.

13. A method of claim 1 wherein said bottom electrode comprises a platinum-rhodium alloy.

14. A method of claim 1 wherein said tantalum pentoxide layer is formed by chemical vapor deposition.

15. A method of claim 1 wherein said tantalum pentoxide layer has a thickness of about 50 to about 150 Angstroms.

16. A method of claim 15 wherein said tantalum pentoxide layer has a thickness of about 100 Angstroms.

17. A method of claim 1 wherein said upper electrode is formed by physical vapor deposition.

18. A method of claim 1 wherein said upper electrode comprises platinum.

19. A method of claim 1 wherein said upper electrode comprises rhodium.

20. A method of claim 1 wherein said upper electrode comprises a platinum-rhodium alloy.

21. A method for making an integrated circuit capacitor comprising:

forming a bottom electrode over an oxidizable conductive plug;

forming a tantalum pentoxide layer over said bottom electrode;

annealing said tantalum pentoxide layer in a nitrogen atmosphere at a temperature of about 650° C to about 900° C;

annealing said tantalum pentoxide layer in an ozone atmosphere at a temperature of about 25° C to about 550° C; and

forming an upper electrode over said tantalum pentoxide layer.

22. A method of claim 21 wherein said nitrogen anneal is performed while maintaining a temperature of about 675° C.

23. A method of claim 21 wherein said ozone anneal is performed while maintaining a temperature of about 475° C.

24. A method of claim 21 wherein said nitrogen anneal precedes said ozone anneal.

25. A method of claim 21 wherein said ozone anneal precedes said nitrogen anneal.

26. A method of claim 21 further comprising forming a diffusion barrier between said oxidizable conductive plug and said bottom electrode.

27. A method of claim 26 wherein said diffusion barrier comprises tantalum nitride.

28. A method of claim 26 wherein said diffusion barrier comprises tantalum silicon nitride.

29. A method of claim 26 wherein said diffusion barrier comprises titanium nitride.

30. A method of claim 21 wherein said bottom electrode is formed by chemical vapor deposition.

31. A method of claim 21 wherein said bottom electrode comprises platinum.

32. A method of claim 21 wherein said bottom electrode comprises rhodium.

33. A method of claim 21 wherein said bottom electrode comprises a platinum-rhodium alloy.

34. A method of claim 21 wherein said tantalum pentoxide layer is formed by chemical vapor deposition.

35. A method of claim 21 wherein said tantalum pentoxide layer has a thickness of about 50 Angstroms to about 150 Angstroms.

36. A method of claim 35 wherein said tantalum pentoxide layer has a thickness of about 100 Angstroms.

37. A method of claim 21 wherein said upper electrode is formed by physical vapor deposition.

38. A method of claim 21 wherein said upper electrode comprises a platinum layer.

39. A method of claim 38 wherein said platinum layer is formed by chemical vapor deposition.

40. A method of claim 21 wherein said upper electrode comprises a rhodium layer.

41. A method of claim 40 wherein said rhodium layer is formed by chemical vapor deposition.

42. A method of claim 21 wherein said upper electrode comprises a platinum-rhodium alloy layer.

43. A method of claim 42 wherein said platinum-rhodium alloy layer is formed by chemical vapor deposition.

44. A method of forming an integrated circuit comprising:

forming an insulating layer over a semiconductor substrate;

forming a oxidizable conductive plug in said insulating layer;

forming a second insulating layer over said oxidizable conductive plug and said insulating layer;

forming an opening in said second insulating layer, said opening being over said oxidizable conductive plug;

forming a diffusion barrier layer in said opening and over said oxidizable conductive plug;

forming a bottom electrode over said diffusion barrier layer;

forming a tantalum pentoxide layer over said bottom electrode;

annealing said tantalum pentoxide layer in a nitrogen atmosphere;

annealing said tantalum pentoxide layer in an ozone atmosphere; and

forming an upper electrode over said tantalum pentoxide layer.

45. A method of claim 44 wherein said ozone atmosphere anneal is performed at a temperature which does not increase the resistance of said oxidizable conductive plug by more than about 50% over its initial resistance.

46. A method of claim 44 wherein said insulating layer comprises borophosphosilicate glass.

47. A method of claim 44 wherein said oxidizable conductive plug comprises polycrystalline silicon.

48. A method of claim 44 wherein said second insulating layer comprises borophosphosilicate glass.

49. A method of claim 44 wherein said diffusion barrier comprises tantalum nitride.

50. A method of claim 44 wherein said diffusion barrier comprises tantalum silicon nitride.

51. A method of claim 44 wherein said diffusion barrier comprises titanium nitride.

52. A method of claim 44 wherein said bottom electrode comprises platinum.

53. A method of claim 44 wherein said bottom electrode comprises rhodium.

54. A method of claim 44 wherein said bottom electrode comprises a platinum-rhodium alloy.

55. A method of claim 44 wherein said tantalum pentoxide layer is formed by chemical vapor deposition.

56. A method of claim 44 wherein said tantalum pentoxide layer has a thickness of about 50 to about 150 Angstroms.

57. A method of claim 56 wherein said tantalum pentoxide layer has a thickness of about 100 Angstroms.

58. A method of claim 44 wherein said upper electrode is formed by physical vapor deposition.

59. A method of claim 44 wherein said upper electrode comprises a platinum layer.

60. A method of claim 59 wherein said platinum layer is formed by chemical vapor deposition.

61. A method of claim 44 wherein said upper electrode comprises a rhodium layer.

62. A method of claim 61 wherein said rhodium layer is formed by chemical vapor deposition.

63. A method of claim 44 wherein said upper electrode comprises a platinum-rhodium alloy layer.

64. A method of claim 63 wherein said platinum-rhodium alloy layer is formed by chemical vapor deposition.

65. An integrated circuit capacitor comprising:

a bottom electrode formed over a conductive plug, said bottom electrode comprising at least one of a platinum, rhodium, and a platinum-rhodium alloy layer;

a nitrogen and oxygen annealed tantalum pentoxide layer formed over said bottom electrode, said annealed tantalum pentoxide having crystal growth primarily in the <200> direction; and

an upper electrode formed over said tantalum pentoxide layer, said upper electrode comprising at least one of a platinum, rhodium, and a platinum-rhodium alloy layer.

66. The capacitor of claim 65 wherein said capacitor further comprises a diffusion barrier between said conductive plug and said bottom electrode.

67. The capacitor of claim 66 wherein said diffusion barrier comprises tantalum nitride.

68. The capacitor of claim 66 wherein said diffusion barrier comprises tantalum silicon nitride.

69. The capacitor of claim 66 wherein said diffusion barrier comprises titanium nitride.

70. The capacitor of claim 65 wherein said tantalum pentoxide layer is formed by chemical vapor deposition.

71. The capacitor of claim 65 wherein said tantalum pentoxide layer has a thickness of about 50 to about 150 Angstroms.

72. The capacitor of claim 71 wherein said tantalum pentoxide layer has a thickness of about 100 Angstroms.

73. The capacitor of claim 65 wherein said upper electrode is formed by physical vapor deposition.

74. The capacitor of claim 65 wherein said upper electrode is formed by chemical vapor deposition.

75. An integrated circuit capacitor comprising:

a bottom electrode formed over a conductive plug, said bottom electrode comprising at least one of a platinum, rhodium, and a platinum-rhodium alloy layer;

a nitrogen and oxygen annealed tantalum pentoxide layer formed over said bottom electrode, said annealed tantalum pentoxide having crystal growth primarily in <001> direction; and

an upper electrode formed over said tantalum pentoxide layer, said upper electrode comprising at least one of a platinum, rhodium, and a platinum-rhodium alloy layer.

76. The capacitor of claim 75 wherein said capacitor further comprises a diffusion barrier between said conductive plug and said bottom electrode.

77. The capacitor of claim 76 wherein said diffusion barrier comprises tantalum nitride.

78. The capacitor of claim 76 wherein said diffusion barrier comprises tantalum silicon nitride.

79. The capacitor of claim 76 wherein said diffusion barrier comprises titanium nitride.

80. The capacitor of claim 75 wherein said tantalum pentoxide layer has a thickness of about 50 to about 150 Angstroms.

81. The capacitor of claim 80 wherein said tantalum pentoxide layer has a thickness of about 100 Angstroms.

82. An integrated circuit capacitor comprising:

A bottom electrode formed over an oxidizable polycrystalline silicon plug, said polycrystalline silicon plug having an initial resistance value;

an annealed tantalum pentoxide dielectric formed over said bottom electrode;

an upper electrode formed over said tantalum pentoxide dielectric, wherein said oxidizable polycrystalline silicon plug has a post-anneal resistance value which is no more than fifty percent higher than said initial resistance value.

83. The capacitor of claim 82 wherein said capacitor further comprises a diffusion barrier between said oxidizable polycrystalline silicon plug and said bottom electrode.

84. The capacitor of claim 83 wherein said diffusion barrier comprises tantalum nitride.

85. The capacitor of claim 83 wherein said diffusion barrier comprises tantalum silicon nitride.

86. The capacitor of claim 83 wherein said diffusion barrier comprises titanium nitride.

87. The capacitor of claim 82 wherein said tantalum pentoxide layer is formed by chemical vapor deposition.

88. The capacitor of claim 82 wherein said tantalum pentoxide layer has a thickness of about 50 to about 150 Angstroms.

89. The capacitor of claim 88 wherein said tantalum pentoxide layer has a thickness of about 100 Angstroms.

90. The capacitor of claim 82 wherein said upper electrode is formed by physical vapor deposition.